

ABOUT THE DYNAMICS OF SOME METHODS OF INTEGRATING CONVERSION OF ANALOG SIGNAL INTO DIGITAL CODE*

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The new principles of constructing of the clocked reversible integrating analog-to-digital converters (ADCs) with pulse-width (PWM) and in-phase amplitude-frequency-pulse modulation (AFPM), as well as closed integrating ADC with tactless bit-by-bit equilibration is considered. The block diagrams and time diagrams of the ADC are reduced. An analysis of their dynamic characteristics is given.

It is shown that the expansion of bandwidth of the ADC with PWM is possible by increasing the number of cycles of sweep conversion "within" the synchronization interval. In particular, it is proved the ADC with in-phase AFPM in comparison with the known technical solutions has at least an order higher temperature and time stability of the characteristics. The bandwidth of the closed integrating ADC with tactless bit-by-bit equilibration depends on the time constant of channel integration. Significant expansion of the ADC bandwidth which purchased due to the reducing of the metrological characteristics is possible in his open-loop structure in the deficiency of channel integration.

Keywords: integrating analog-digital converter, integrating sweep converter, voltage converter into frequency of pulses, pulse-width modulation, amplitude-frequency-pulse modulation, tactless bit-by-bit equilibration, noise immunity, control system.

Introduction

In control systems (CS) with the slave network of power valve converters (VC) [1–4] limit bandwidth f_b is determined by the frequency f_s and the number "m" of phase power supply and according to A. Kotelnikov theorem is $f_b \leq 0,5 \cdot m \cdot f_s$ [5]. Under these conditions, the clock frequency removal of data from analog-to-digital converters (ADCs) to choose the higher of those values that are dictated by the discreteness of VC is not only pointless, but harmful, so as it leads to a decrease in noise-immunity of control system due to "entering" of high-frequency pulsation [6] determined by the properties of the converted analog signal into a digital code. These coordinates are, for example, the signals of the current and voltage feedback, and in some cases, the rate of the actuating mechanism, as well as external noises, which are often the generator directly to the elements of the electronic part of the CS, working in a discrete (pulsed) mode [7]¹.

To date, more effective ways to increase the noise immunity of the ADC than integrating analog-digital conversion, not invented. The leaders are ADC with push-pull integration [8, 9], the ADC with integrating pulse-width modulation (PWM) [10] and number-to-pulse ADC [9].

The basic disadvantage of the ADC with push-pull integration is interval when the ADC's input is disconnected from the source of the converted signal

and the CS is actually loses connection with the processes that occur in it. The only way to avoid a similar situation is used in a bundle of two antiphase running the ADC, which complicates not only the whole construction of the ADC, but also its setting.

The basis of the ADC with PWM are integrating sweep converters (SC), which synchronized external sawtooth or pulse signal. The processes in these ADCs are aperiodic mode, depending on the parameters of the synchronization signal and the time constant of SC's integration circuit [11] and, as a rule, are rather inertial, to be used in fast CS.

In the number-pulse ADC are made rigid requirements on the work stability of the converter of input signal into frequency of pulses, which added task of supplying the reversibility of the ADC that is his ability to work with the signals of both positive and negative polarity.

The overall quality of the referred ADCs is open character of their structure, which gives to rise the natural problem of providing a high level of metrological characteristics of the converter, and the need for clock interval of the ADC, after which the command is issued to permit data reading. Often the clock period is dictated by the most inertial link of the ADC, which determines the dynamics of this method of analog-digital conversion. Usually, when solving the traditional problems of automation, the fact of the ADC

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clock is not negative, in some cases, it is an effective means of suppressing noise [7]. However, optimization of dynamic characteristics of objects with non-stationary parameters and a high level of external noise is desirable to have the tactless integrating ADC, allowing the system to change the sampling frequency, depending on its mode.

The purpose of the article is acquaintance of specialists in the field of information electronics and automation of technological processes, as well as the manufacturers of integrated circuits with the developments in the field of ADCs, which have been made in recent years in the department of electric driver of SUSU and are intended for control systems by valve

electric drives and technology automation [12–14], characterized by high levels of interfering signals.

Clocked ADC with integrating PWM

ADC (Fig. 1 a) contains the SC, the generator of signal of sawtooth sweep GSS and converter "PWM – DIGIT".

The SC [11] includes an adder Σ , an integrator with a transfer function $W(p) = 1/T_I p$, where T_I is time constant and the anhysteresis relay element RE with symmetric no inverting characteristic, the output signal which varies discretely within $\pm A$.

"Inside" the GSS of a counting circuit (in fig.1 a isn't shown) is formed digital reference sawtooth

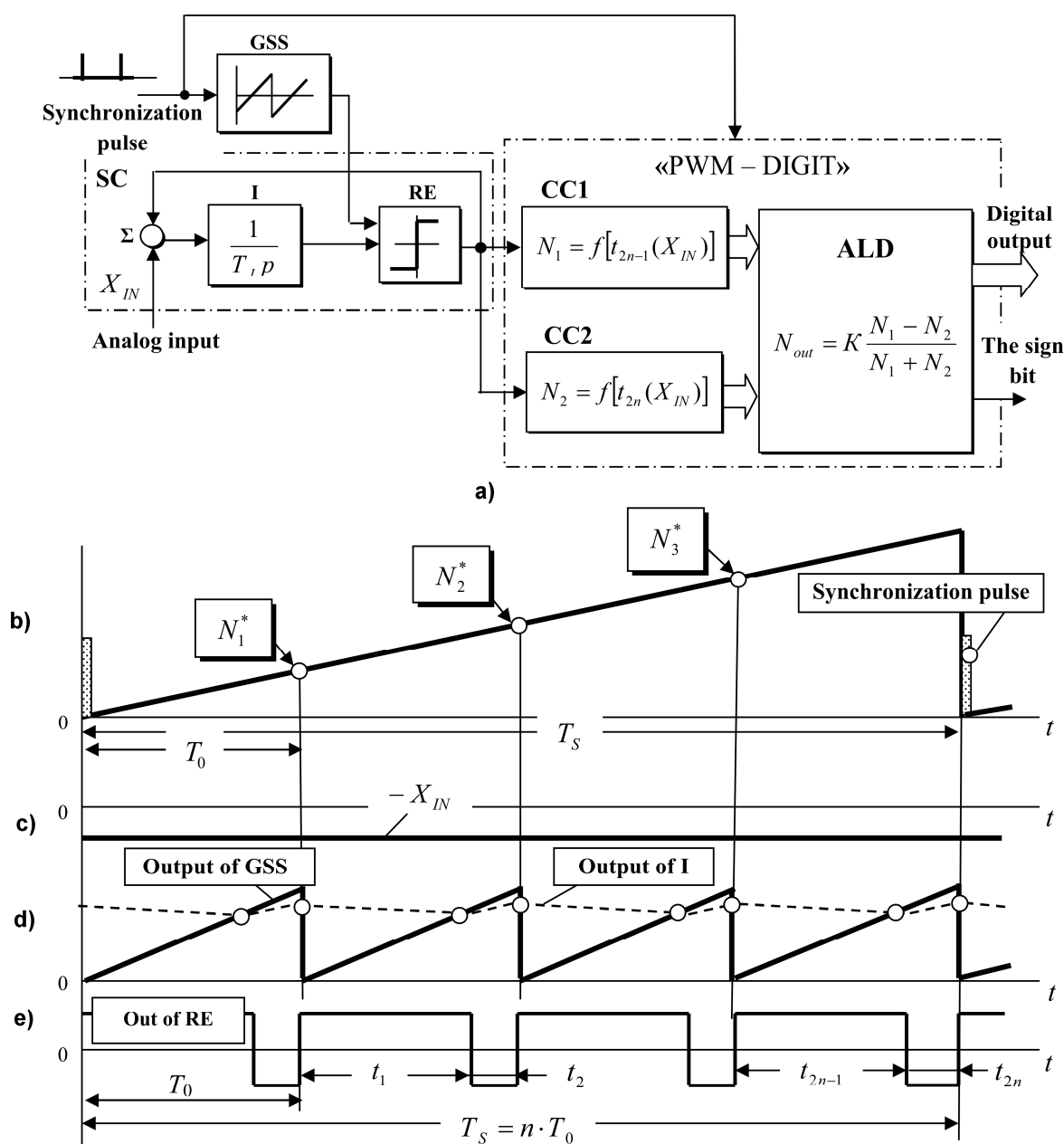


Fig. 1. Block diagram (a) and timing diagrams of signals (b – e) of the reverse integrating analog-to-digital converter with a PWM

sweep (Fig. 1 b), period T_S of which is determined by the external clock pulses corresponding to the sampling interval of the VC.

The discreteness of reference sweep is determined by the frequency of own generator of counting pulses and is negligible quantity. With help the sweep are given numbers $N_1^*, N_2^*, N_3^*, \dots, N_k^*$ so that they followed with a period $T_0 < T_S$, where $T_S / T_0 = n -$ an integer. In Fig. 1 b as an example, there are three values N_1^*, N_2^*, N_3^* , which form a discrete front of GSS's output analog sweep destined for synchronization of SC.

Switching the REs occurs at instant times, when equal amplitudes of the signals of the master sweep to the GSS's output and slave sweep from the output of the integrator I. If the input signal X_m is, for example, negative polarity (Fig. 1 c), then on the time interval t_1 the signal of the master sweep from the output of the integrator I equal difference of the signal at the output of RE and the input signal of SC ($A - X_m$), and in the interval t_2 it equal add of these signals ($-A - X_m$) (Fig. 1 c, e).

As a result, $t_1 > t_2$, and the average value of the output pulses of REs is proportional to the input signal X_{in} . With the positive input signal SC works similarly with the only difference is that $t_1 < t_2$.

In general, the SC synchronized of "saw" on the output of RE is an aperiodic link $W(p) = 1 / (1 + T_E p)$ [11], where $T_E \approx 0,45 \cdot \bar{T}_I \cdot T_0$ is the equivalent time constant of the SC; $\bar{T}_I = T_I / T_{GSS}$ is normalized value of the integrator time constant I referred to the time constant of the signal of sawtooth sweep T_{GSS} . In general, $T_0 = T_S / n$, where n is the division factor of synchronization interval T_S (Fig. 1 b – e). At that, the condition $T_I > 2T_{GSS}$ should comply for reliable synchronization of SC by signal from the output of GSS.

From these relations it is clear that as the period of the sawtooth sweep signal T_0 "inside" synchronization interval decreases so speed of SC increases.

Converter "PWM – DIGIT" (Fig. 1 a) contains two counting channels CC1, CC2 and arithmetic-logic device ALD. CC1 converts into a digital code N_1 pulses of positive polarity, and CC2 forms a code of N_2 , depending on the duration of the output pulses of negative polarity.

In this case, are the following options of "numbering" of the PWM signal from the output of the SC.

In the first case it is assumed that on the interval T_S (Fig. 1 b) sum of "odd" $N_1 \equiv \sum_{i=1}^n t_{2i-1}$ and "even"

$N_2 \equiv \sum_{i=1}^n t_{2i}$ synchronization intervals of SC (Fig. 1 d)

are converted to "digit" with following calculation of the output code $N_{OUT} = K \frac{N_1 - N_2}{N_1 + N_2}$, where K is the coefficient of scheme proportionality.

The second option of converting of analog signal into the code takes into account only the latest in a

series of periods when $N_1 \equiv t_{2n-1}$, $N_2 \equiv t_{2n}$ and $N_{OUT} = K \frac{N_1 - N_2}{N_1 + N_2}$. In either case, the sign bit is

formed in ALD by comparing the values of N_1 and N_2 .

In Fig. 2 shows the logarithmic amplitude-frequency characteristics (LAFC) $k = F(\bar{f})$ of ADC with PWM, taken at different values of the division factor $n = T_S / T_0$ of the synchronization interval T_S and the relative integration time constant of SC $\bar{T}_I = 2,2$ for the first (Fig. 2 a) and the second (Fig. 2 b) algorithms of "numbering" of the PWM signal are "inside" of the synchronization interval T_S . Here, k is a coefficient of transmission of an integrating ADC; $\bar{f} = f_{IN} / f_S$ is normalized frequency f_{IN} of the harmonic input signal divided by the frequency of clock pulses $f_S = (T_S)^{-1}$ ($T_S = 3,3$ ms). LAFC obtained by modeling of the ADCs in a technical computing software MatLab + Simulink.

LAFC analysis showed the following:

- an increase in the number "n" sampling intervals T_0 "inside" the synchronization interval T_S of VC leads to the expansion of ADC's bandwidth due to the to reduce the equivalent time constant of the T_E of SC (Fig. 2 a). For example, for $n = 1$ a range of uniform bandwidth of ADCs frequency is at the level $\bar{f} \approx 0,17$ and for $n = 8$ is $\bar{f} \approx 0,4$;

- slight difference between the LAFCs for $n = 4$ and $n = 8$ shows that the rational value of the coefficient "n" be considered as $n = 4$, when a compromise is possible between the dynamics and noise-immunity of the ADC;

- "numbering" of the PWM signal from a finite sampling interval a series of SC's output pulses (Fig. 2 b) can increase the bandwidth of the ADC as compared to the initial method of converting of PWM signal into a digital code (Fig. 2 a). For example, if the "numbering" is not a series of pulses, but only a finite sampling interval (period), then for $n = 4$ bandwidth of the ADC (Fig. 2 a) increases almost to the limit value $\bar{f} \approx 0,5$ (Fig. 2 b).

This is explained as follows. So under the influence of the input step waveform (Fig. 3 a), SC goes on the desired trajectory to exponentially when each of the sampling intervals $T_{01} \dots T_{0n}$ (Fig. 3 b) contains the error $\Delta_1 \dots \Delta_n$ (Fig. 3 c). Obviously, the error of the last of a series of sampling intervals will be the lowest in comparison, for example, with an average resulting error of the SC $[\delta = (\sum \Delta_i) / n] > \Delta_n$ for the entire sampling interval T_S of VC.

Clocked ADC with in-phase amplitude-frequency-pulse modulation (AFPM)

This class of ADCs [15] is advisable to apply in cases where a wide dynamic range of the converted

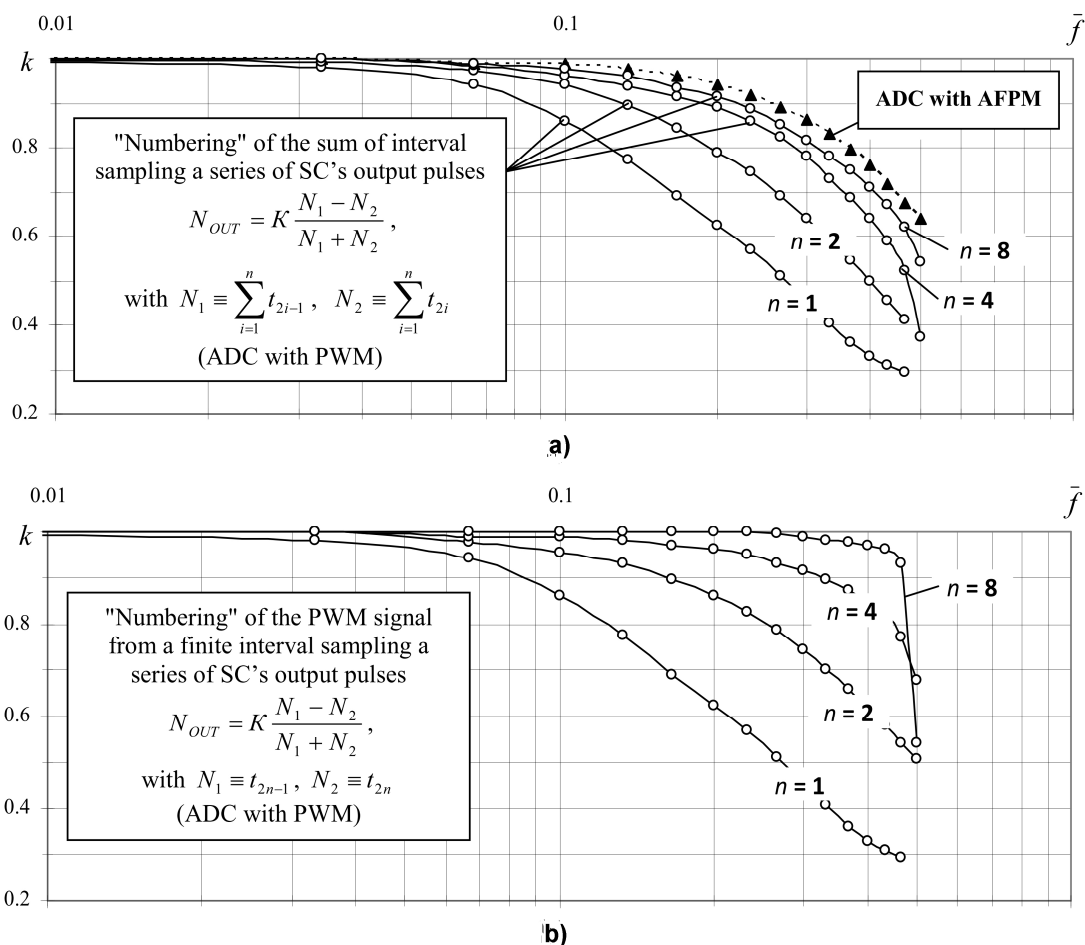


Fig. 2. The logarithmic amplitude-frequency characteristics (LAFC) $k = F(\bar{f})$ of integrating ADC with PWM in different ways of 'numbering' of PWM signal (a, b) and LAFC of ADC with in-phase AFPM

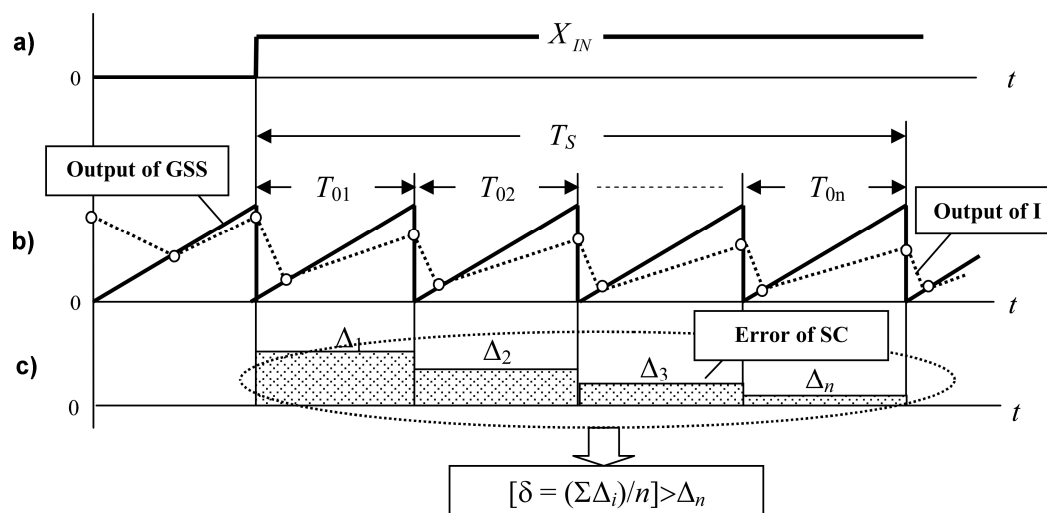


Fig. 3. The timing diagrams of signals to the analysis of the error of ADC with PWM

signal must be combined with high temperature stability characteristics of the analog-digital converter.

ADC (Fig. 4 a) contains two identical on his action integrating a voltage converter into frequency of pulses VCF1 and VCF2 [16, 17], containing amplitude modulators AM1, AM2, adders $\Sigma 1$, $\Sigma 2$, integrators I1, I2 and relay elements RE1, RE2.

Each of the VCF is intended for work with the signal of a certain polarity. So VCF1 transforms the input voltage of positive polarity into frequency of pulses, and VCF2 transforms input signal of negative polarity.

In the absence of a signal X_{IN} on the ADC's information input (Fig. 4 b), the output voltage of AM1

and AM2 are zero, so the blocks $\Sigma 1$, I1, RE1 and $\Sigma 2$, I2, RE2 operate in a free-running mode when the outputs of RE1 (Fig. 4 d) and RE2 (Fig. 4 e) are formed bipolar pulses with frequency $f_0 = (T_0)^{-1}$. If links characteristics of channels VCF1, VCF2 are identity, then its work with an equal value of the initial frequency f_0 .

A possible phase shift between output signals of VCF1 and VCF2 principle does not matter, since it might ultimately lead to a conversion error only to one significant digit of binary code.

The output signals of the integrators I1, I2 are symmetric sawtooth wave shape and are limited in amplitude of switching thresholds $\pm b$ of RE1 and RE2 (Fig. 4 d, e).

When applied to the ADC input signal is positive (Fig. 4 b) then at the input of AM1 appears positive sign voltage, which is then converted into frequency of output pulses of RE1, which increases in proportion to the amplitude of the X_{IN} due to in-phase of output

pulses of AM1 and RE1 (in-phase AFPM) (Fig. 4 c, d). At the same time VCF2 works in a free-running mode with an initial frequency equal f_0 , acting as a channel of the reference frequency.

In general relations (1) are valid for VCF1 and VCF2.

$$\begin{cases} t_{2n-1} = t_{2n} = 0,5T_0/(1 + \bar{X}_{IN}); \\ T_{0,n} = t_{2n-1} + t_{2n} = 0,5T_0/(1 + \bar{X}_{IN}); \\ T_0 = T_{0,n}|_{X_{IN}=0} = 4\bar{b}T_I; \bar{f}_{OUT} = T_0/T_{0,n} = 1 + \bar{X}_{IN}; \\ \bar{b} = |b/A|; \bar{X}_{IN} = |X_{IN}/A|; n = 1, 2, 3, \dots \end{cases} \quad (1)$$

where \bar{f}_{OUT} – the normalized frequency of the output pulses of VCF1 and VCF2 respectively; \bar{X}_{IN} , \bar{b} – the normalized value of the ADC input signal and switching thresholds $\pm b$ of RE1, RE2, respectively; T_I – time constant of the integrators I1, I2; $\pm A$ – the amplitude of the output pulses of RE1, RE2. At the same time $\bar{b} < 1,0$ and the value of \bar{X}_{IN} can be arbitrary.

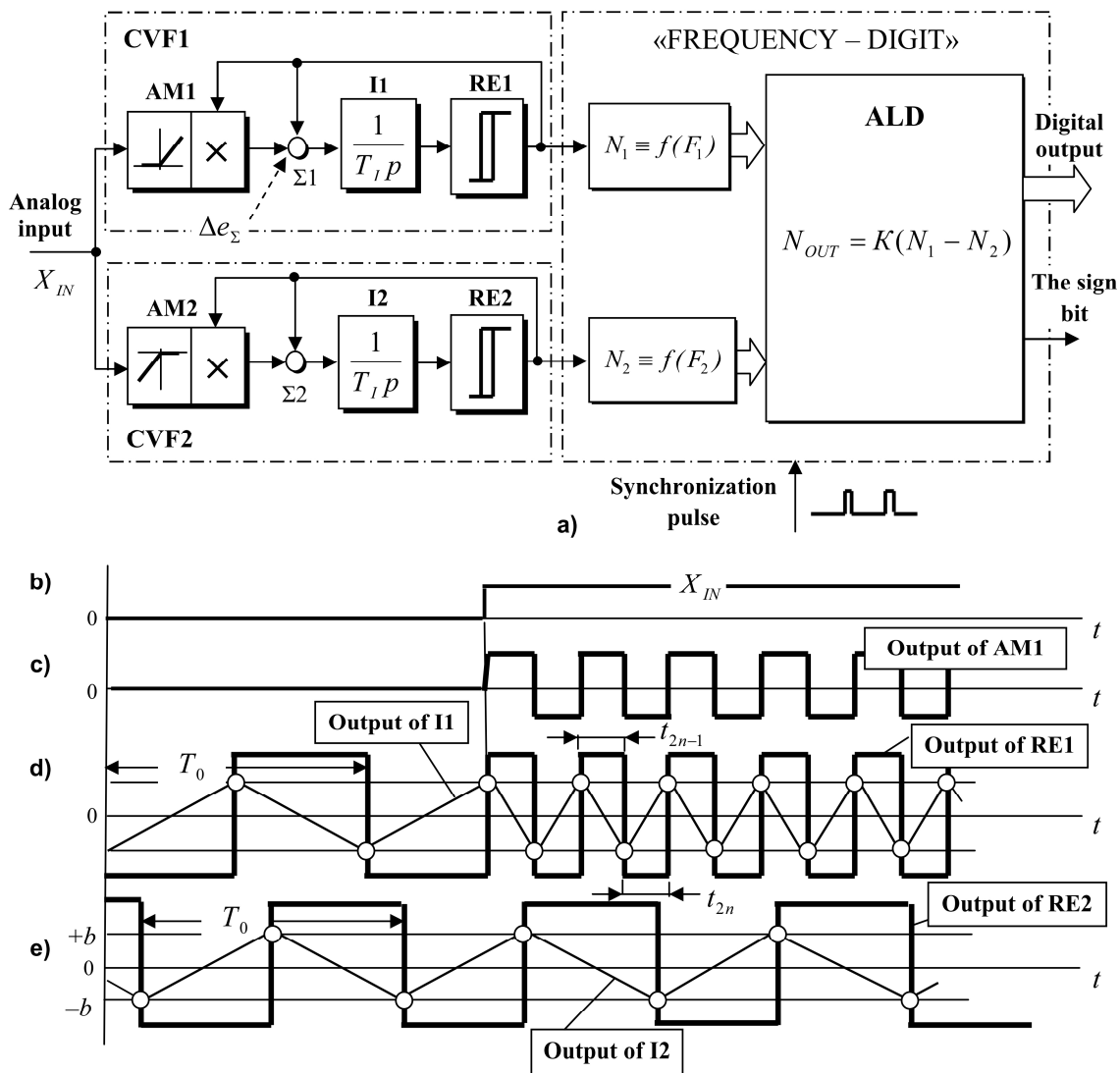


Fig. 4. Block diagram (a) and timing diagrams of signals (b – e) of the reverse integrating ADC with in-phase AFPM

trarily large from the theoretical positions, as well as the frequency of the output pulses of VCF.

Further transformation of impulses frequency into a digital code is done using the channel "FREQUENCY – DIGIT" (Fig. 4 a), where CC1 forms the number of N_1 , proportional to the frequency of the output pulses of VCF1 and CC2 forms the number of N_2 , depending on the frequency of the output signal of VCF2.

The resulting code of ALU $N_{OUT} = K \cdot (N_1 - N_2)$ is passed to output buses of the ADC at time of formation of the synchronization pulse and saved on them until the end of the next conversion cycle. Sign bit is also obtained by comparing the values of N_1 and N_2 .

Analysis of dynamic characteristics of the ADC with AFPM showed that the determining factor here is the frequency of synchronization pulses, and from the frequency of self-oscillations of VCF1, VCF2 depends only on the ADC's digit, that is, the sampling error on the level of the converted signal.

Logarithmic amplitude-frequency characteristics of the ADC with AFPM is shown in Fig. 2 a, which was read at an initial frequency of the output pulses of VCF1, VCF2 equal to $f_0 = 10$ kHz. The results show that the dynamic property, this class of the ADC, occupies an intermediate position between the ADC-PWM with an integer division of the sampling interval (Fig. 2 a) and ADC-PWM, where the "numbering" is made on the last sampling interval of SC (Fig. 2 b).

The using of VCF with in-phase AFPM can significantly improve the temporal and thermal stability of characteristics of the ADC.

So in the case drift of "zero" signal Δe_Σ of I or AM, for example, positive polarity (relations (2)), the interval t_{2n-1} (Fig. 2) of the output pulses of RE1 is reduced, and the interval t_{2n} is increasing. In this case the resulting error Δf_{OUT}^e of the frequency of output pulses is proportional to $\Delta \bar{e}_\Sigma^2$, while for the traditional structures of VCF [10] is $\Delta f \equiv \Delta \bar{e}$

$$\left\{ \begin{aligned} t_{2n-1}^e &= \frac{2\bar{b}T_I}{1 + \bar{X}_{IN} - \Delta \bar{e}_\Sigma}; \quad t_{2n}^e = \frac{2\bar{b}T_I}{1 + \bar{X}_{IN} + \Delta \bar{e}_\Sigma}; \\ f_{OUT}^e &= (t_{2n-1}^e + t_{2n}^e)^{-1} = \frac{1 + \bar{X}_{IN}}{4\bar{b}T_I} \cdot \left[1 - \frac{\Delta \bar{e}_\Sigma^2}{(1 + \bar{X}_{IN})^2} \right]; \\ \delta f_{OUT}^e &= 1 - \frac{f_{OUT}^e}{f_{OUT}(\Delta \bar{e}_\Sigma=0)} = \frac{\Delta \bar{e}_\Sigma^2}{(1 + \bar{X}_{IN})^2}; \\ \Delta \bar{e}_\Sigma &= \left| \frac{\Delta e_\Sigma}{A} \right|; \quad \bar{b} = \left| \frac{b}{A} \right|; \quad \bar{X}_{IN} = \left| \frac{X_{IN}}{A} \right|. \end{aligned} \right. \quad (2)$$

The system of equations (2) except for the previously adopted the following notation: $\Delta \bar{e}_\Sigma$ is normalized value of the resulting drift of "zero" signal of the integrator I1 (I2) and the amplitude modulator AM1 (AM2) is provided to input of the adder $\Sigma 1$ ($\Sigma 2$) (Fig.

4 a); δf_{OUT}^e is the relative error of the frequency of output pulses of VCF in the presence of signal Δe_Σ .

Given that $\Delta \bar{e}_\Sigma \ll 1,0$, considered the VCF has the temperature and time stability of characteristics of the at least one order of magnitude greater than the known technical solutions.

As shown by experimental research, when the channels VCF1 and VCF2 based on the same hardware components of a series then their resulting drift of the "zero" is the almost identical in sign and magnitude. Then each of the codes N_1 and N_2 contain the same component of the error of "zero" ΔN , which in practice provides a partial self-correction result of the conversion $N_1 - N_2$.

Closed integrating ADC with tactless bit-by-bit equilibration

The integrating ADC with tactless bit-by-bit equilibration [18–20] with a built in its closed circuit digital-to-analog converter (hereinafter "ADC – DAC") (Fig. 5) contains adders $\Sigma_{IN}, \Sigma_{2n-1} \dots \Sigma_{2n-3}$ and Σ_{OUT} , integrator I, relay elements RE1 ... RE n and proportional links P1 ... P n . When considering the principle of the ADC–DAC is limited to four digits "n" of binary code.

Links $\Sigma_{IN}, \Sigma_{2n-1}, \dots, \Sigma_{2n-3}, I, RE1 \dots RE_n$ combine to form the ADC. Functions of the DAC operates the proportional links P1 ... P n and Σ_{OUT} . Adders $\Sigma_{IN}, \Sigma_{2n-1} \dots \Sigma_{2n-3}$ have a unit coefficient of transmission for each of the inputs and produce the subtraction of input signals. The relay elements RE1 ... RE n generally have symmetrical with respect to "zero" hysteresis loop, and their output signal changes discretely within $\pm A$.

The adder Σ_{OUT} has "n" number of inputs with a unit coefficient of transmission for each of them and makes a summation of the signals. Number of inputs the adder is chosen equal to the number of digits "n" of the converted binary code.

Proportional links P1 ... P n are implemented with coefficient of transmission, which are varied according to bit's weight of the converted code in the general case with arbitrary base, but more often, as taken here, with a binary code which is the proportional to series $2^{n-1}, 2^{n-2}, \dots, 2^0$. The largest coefficient of proportional link 2^{n-1} corresponds to the weight of high-order bit of binary code, and the lowest 2^0 corresponds to the weight of lower order bit.

Further in the text use the following notation: Y_I is the output signal of the integrator I, Y_{OUT} is the output signal of the adder Σ_{OUT} ; $\pm A \cdot 2^{n-1}, \pm A \cdot 2^{n-2}, \pm A \cdot 2^{n-3}, \dots, \pm A \cdot 2^0$ are the maximum levels of output signals of proportional links P1 ... P n , respectively; $\pm b$ are switching thresholds of RE1 ... RE n , with $|b| < |A|$; $\pm A$ is the amplitude of the output pulses of the relay elements RE1 ... RE n , and believe that the level "+A" corresponds to a logical "1", and the level "-A" corresponds to a logical "0"; $Q_{n-1}, Q_{n-2}, Q_{n-3}, \dots, Q_0$ are bits of digital output code at the outputs of the RE1 ...

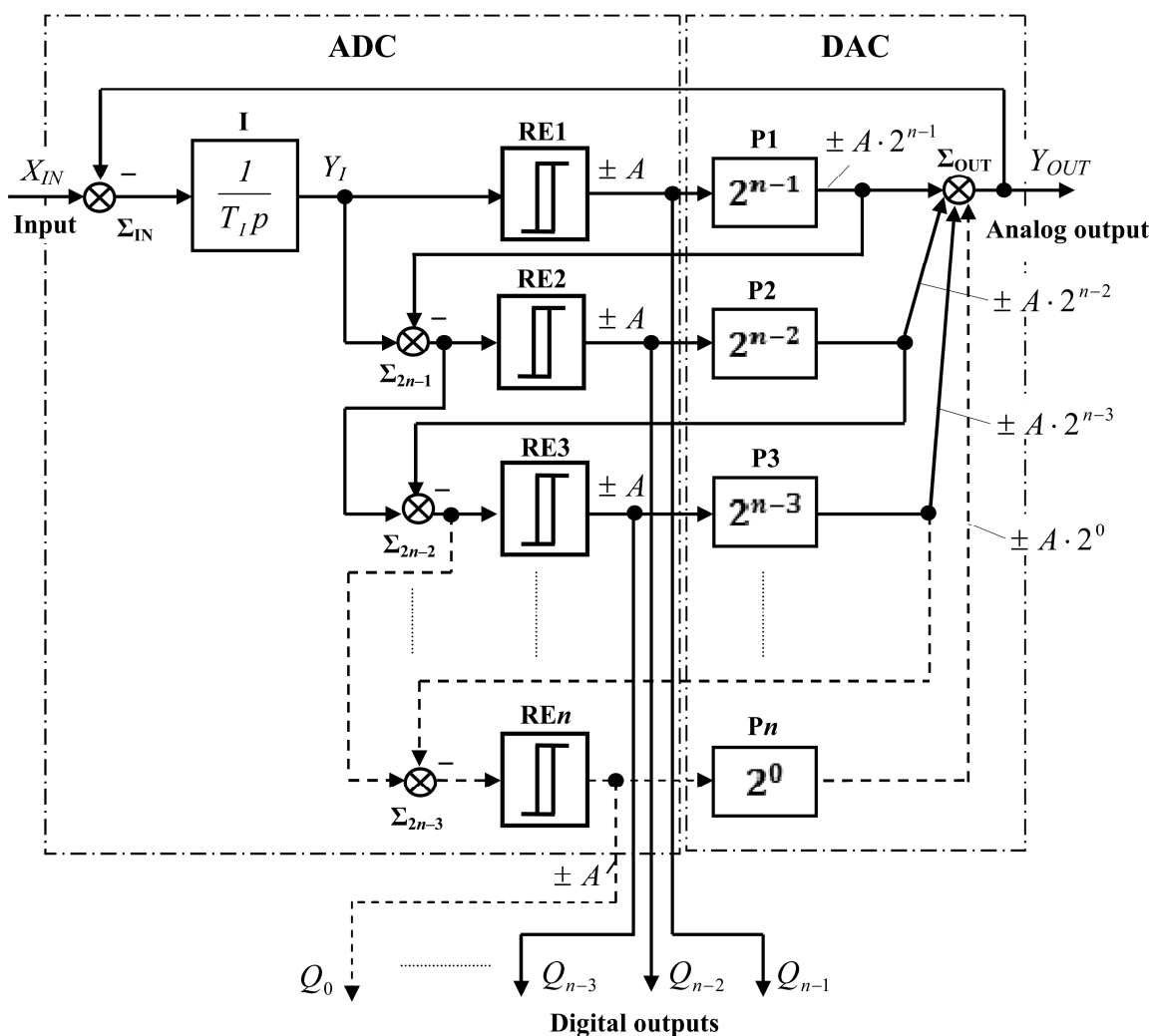


Fig. 5. The block diagram of closed-integrating ADC with tactless bit-by-bit equilibration

RE_n; N₁ is digital code at the output of the RE1 ... RE_n.

For ADC – DAC input signal can be represented in the form of expression $X_{IN} = \pm \Delta(k + 0,5m)$, where $\Delta = 2A_{max}/N_{max} = 2A$ is the weight of the unit of lower-order bit of the converted code in analog form;

$$N_{max} = \sum_{i=0}^{i=n-1} 2^i = 2^n - 1$$

is the maximum value of a binary digital code in decimal, which is formed at the outputs of RE1 ... RE_n; $A = A_{max}/N_{max}$ is the pulse's amplitude at the output of relay elements RE1 ... RE_n, A_{max} is the maximum amplitude of the output signal of the DAC $k = 0, 1, 2, \dots, (N_{max} - 1)/2$ are whole numbers, corresponding decimal numbers of the converted code; m is coefficient taking into account changes of the input signal in the interval Δ ($-1,0 \leq m \leq 1,0$).

Consider the operation of the device, provided $X_{IN} = 0$, when numbers $k = 0$ and $m = 0$.

We assume that the relay element RE1, which forms the high-order bit of the converted code is in the

+A. Then the amplitude on the output of proportional link P1 is $A \cdot 2^{n-1}$. For the equality $X_{IN} = Y_{OUT}$, all the rest RE2 ... RE_n in the system are forced to switch to the "negative" position when the summary output signal Σ_{OUT} is $Y_{OUT} = A(2^{n-1} - 2^{n-2} - 2^{n-3} - \dots - 2^0) = -A$.

The condition that $X_{IN} = Y_{OUT}$ is impossible for the case $X_{IN} = 0$, so that the signal at the output of the integrator I will fall under the action of voltage $-A$ from the output Σ_{IN} , and where the equality $Y_I = -b$ is achieved then first RE1 goes into "negative" state, and RE2 ... RE_n go in "+A". As a result, the summary output signal Σ_{OUT} corresponds a value $Y_{OUT} = A(-2^{n-1} + 2^{n-2} + 2^{n-3} - \dots + 2^0) = -A$.

Thus, for $X_{IN} = 0$ ADC – DAC is always in the mode switch of all relay elements with carrier oscillation frequency $f_0 = 1/(4\bar{b}T_I)$, where $\bar{b} = |b/A|$ is the normalized value of switching threshold of RE1 ... RE_n; T_I is time constant of integration.

As a result with $X_{IN} = 0$ at the output of RE1 ... RE_n periodically formed two values of shifted binary

code N_1 , which are equal to: $(N_{\max} + 1)/2$ and $(N_{\max} - 1)/2$. To bring it to the standard form necessary from the code value N_1 subtract the value $N_2 = (N_{\max} + 1)/2$. The latter is implemented by the device of subtracting codes (in Fig. 5 is not shown to simplify the circuit ADC – DAC). Then, for $X_{IN} = 0$ the output code of converter $N_3 = N_1 - N_2$ in decimal form will be equal zero or minus one. As a result, the output of the ADC is formed by a static error which is equal to one lower order bit. With a large number of digits of ADC – DAC ($n \geq 8$) the error is almost no noticeable effect on the accuracy of his work and can be neglected.

For other values of $k \neq 0$ and $m = 0$, ADC – DAC works similar to the case with numbers $k = 0$ and $m = 0$. In this case at least one of the relay elements RE1 ... RE n is necessarily in a mode of switching with a carrier frequency $f_0 = 1/(4\bar{b}T_I)$.

Consider the work of the converter for other values of m , different from zero and changing the range $-1,0 < m < 1,0$ and $k = 0$ when $X_{IN} = \pm A \cdot m$. For these values the device goes into a frequency-pulse-width modulation (FPWM), in which the switching frequency of RE1 ... RE n reduced in accordance with the expression $f = f_0 \cdot (1 - m^2)$. The condition code N_1 on the output of RE1... RE n remains the same as for the case $k = 0$ and $m = 0$.

For $m = 1$ and any other integer values of k the switching frequency of RE1 ... RE n becomes equal zero and there is an established process in the converter, when $X_{IN} = Y_{OUT}$. For example, for $X_{IN} = A$ ($k = 0$) the relay element RE1 is switched to "positive" state, and RE2 ... RE n are switched in the "negative" position. As a result, the summary signal at the output of the DAC is $Y_{OUT} = A(2^{n-1} - 2^{n-2} - 2^{n-3} - \dots - 2^0) = A$ and is balanced by the input signal $X_{IN} = A$. The output voltage of the integrator I reaches a steady-state value $Y_I(t) = b$ so as to constantly keep the RE1 in a "positive" state. Offset digital code N_1 at the output of RE1 ... RE n is equal value $(N_{\max} + 1)/2$, and the code $N_3 = 0$.

Similarly, ADC – DAC operates at other values of k and $m = 1$. For example, the maximum possible value $k = (N_{\max} - 1)/2$ will correspond the maximum input signal level $X_{IN} = \pm A \cdot \left(\frac{N_{\max} - 1}{2} + \frac{1}{2}\right) = \pm A \cdot N_{\max}$. If $X_{IN} = A \cdot N_{\max}$, then RE1 ... RE n switched to a state $+A$.

As a result, the summary output signal Σ_{OUT} is equal to $Y_{OUT} = A(2^{n-1} + 2^{n-2} + 2^{n-3} + \dots + 2^0) = A \cdot N_{\max}$ and is balanced of input signal $X_{IN} = A \cdot N_{\max}$. The

output voltage of the integrator I reaches a steady-state value $Y_I(t) = (N_{\max} - 1) + b$ so as to constantly keep RE1 ... RE n in "positive" state, which corresponds to the minimum value of the code $N_1 = 0$. When you subtract from the code N_1 to code $N_2 = (N_{\max} + 1)/2$ we get a code $N_3 = (N_{\max} + 1)/2$ on the converter output.

For $X_{IN} = -A \cdot N_{\max}$, conversely all the RE1 ... RE n are switched in "negative" state, when the output voltage Σ_{OUT} changes sign and becomes, equal $Y_{OUT} = -A(2^{n-1} + 2^{n-2} + 2^{n-3} + \dots + 2^0) = -A \cdot N_{\max}$, which corresponds to the minimum value of the code $N_1 = 0$. When you subtract from code N_1 to code $N_2 = (N_{\max} + 1)/2$ we get a code $N_3 = -(N_{\max} + 1)/2$ on the converter output.

The considered ADC – DAC is a closed system, so the steady-state mode the signal level X_{IN} at the input of ADC must always be balanced by voltage output Y_{OUT} of the DAC. When the digit capacity of DAC does not provide the desired accuracy (discrete) of transformation between levels, then between these levels starting mode of frequency-pulse-width modulation. However, the averaged integral accuracy is always ensured because of the integrator in the direct regulation channel.

In Fig. 6 shows the oscillograms of the four-digit integrating ADC – DAC, obtained on the basis of computer modeling in the program MatLab + Simulink, when exposed to its input the dynamic signal $X_H(t) = A_m \cdot \sin(2\pi f t)$, where A_m, f are the amplitude and the frequency of the harmonic input signal, respectively.

Modeling was performed with the following parameters: the maximum amplitude at the output of the DAC is equal to $A_{\max} = 15$ V, the weight of the unit of lower bit order of converted code in analog form is equal to $\Delta = 2A_{\max}/(2^n - 1) = 2$ V, the amplitude of the pulses at the output of relay elements RE1 ... RE4 are equal to $A = A_{\max}/(2^n - 1) = 1$, normalized switching thresholds of relay elements RE1 ... RE4 are equal to $\bar{b} = |b/A| = 0,5$, integration time constant of the integrator is equal to $T_I = 0,1$ ms, the carrier oscillation frequency $f_0 = 1/(4\bar{b}T_I)$ of converter by $X_{IN} = 0$ is equal to 5 kHz.

From the oscillograms at the Fig. 6 can be seen that the output signal at the output of the DAC is divided into 15 modulation zones ($Z = 2^n - 1$) according to the digit "n" of binary code. Within each modulation zone converter operates in the mode of FPWM, as a result, the average output signal $Y_0(t)$ of DAC with high accuracy reproduces the harmonic input wave-shape $X_H(t)$ (Fig. 6 a, b). With increasing frequency f of input signal the mode of FPWM within each modulation zone disappears and at the device output is formed by a discrete signal (Fig. 6 c, d).

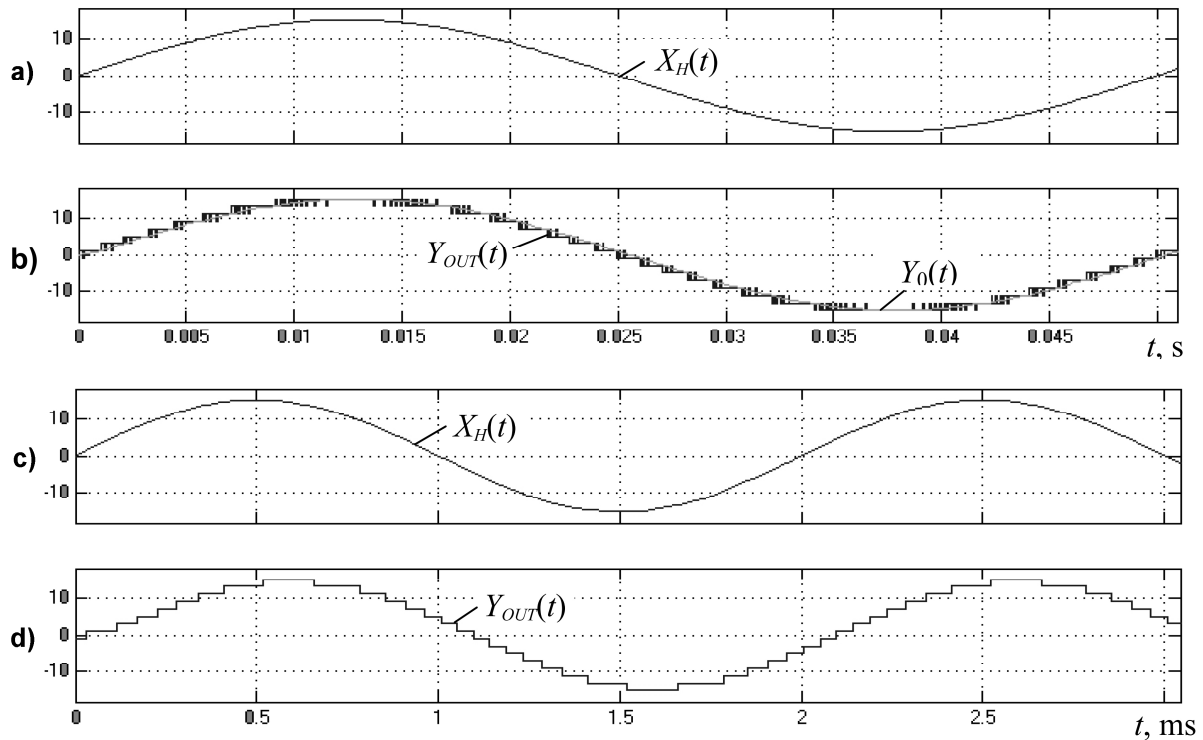


Fig. 6. Oscillograms of the four-digit integrating ADC – DAC with tactless bit-by-bit equilibration with $A_m = 15 \text{ V}$: $f = 20 \text{ Hz}$ (a, b) and $f = 500 \text{ Hz}$ (c, d)

In Fig. 7 shows the logarithmic amplitude-frequency characteristics (L AFC) $k = F(f)$ for the eight-digit integrating ADC – DAC, where $k = A_{OUT} / A_m$ is transfer constant of the ADC – DAC; A_{OUT} is the amplitude of the output signal of the DAC; f is the frequency of the input harmonic signal $X_H(t)$.

Analysis of the results showed that:

- the uniform bandpass f_b of converter "Analog – digit – analog" in which the transmission coefficient k decreases in $\sqrt{2}$ times depends only on the integration time constant T_I and does not depend on the level of the input harmonic signal $X_H(t)$, the switching thresholds "b" of RE1 ... REN and bit "n" of the converter;

- for the chosen value of the normalized switching threshold of RE1 ... REN $\bar{b} = |b/A| = 0,5$ the relative bandwidth of the converter $\bar{f}_b = f_b/f_0$ is approximately 0,32 for all values of the integration time constant T_I (Fig. 7), so that the normalized value of switching thresholds of RE1 ... REN $\bar{b} = |b/A|$ should be chosen as close as possible to the unit, but don't not equal to it. For example, if $\bar{b} = 0,9$ and all values of T_I the relative bandwidth reaches a value $\bar{f}_b \approx 0,57$ that goes beyond the theoretically justified for pulsed systems the extent to which the interface between the frequency range of reliable and delayed sample is determined from Theorem of V.A. Kotelnikov and amounts $\bar{f}_b \leq 0,5$. The results obtained are valid not

only for the eight-bit ADC, but also for the converters with any other digit.

In cases where the priority is the speed of the ADC, but not his noise immunity the integrator I should be replaced by a proportional amplifier (repeater) and the feedback from the output of the DAC to the input of the ADC should be removed.

Findings:

1. At control systems with the slave chain of power valve converters the clock period of integrating ADC with PWM and AFPM advisable to choose a discrete set to VC, which is determined by the number of phase voltage and the configuration of its power circuit.

2. Expanding bandpass of ADC with PWM, clocked synchronization signal of VC, is possible by increasing the number of cycles of the sweeping conversion "inside" of the synchronization interval. In this case the best result gives a method in which the "digitization" is not subject to the amount, and the last of a series of intervals of the sweeping conversion of the ADC on the discretization interval of the VC.

3. ADC with in-phase AFPM has a practically unlimited allowable range of input signal and increased thermal and temporal stability of the characteristics of more than similar solutions for at least an order of magnitude. The dynamic characteristics of this class ADC are determined by sampling interval of VC (cycle transformation).

4. First proposed a closed integrating ADCs with tactless bit-by-bit equilibration and bandwidth

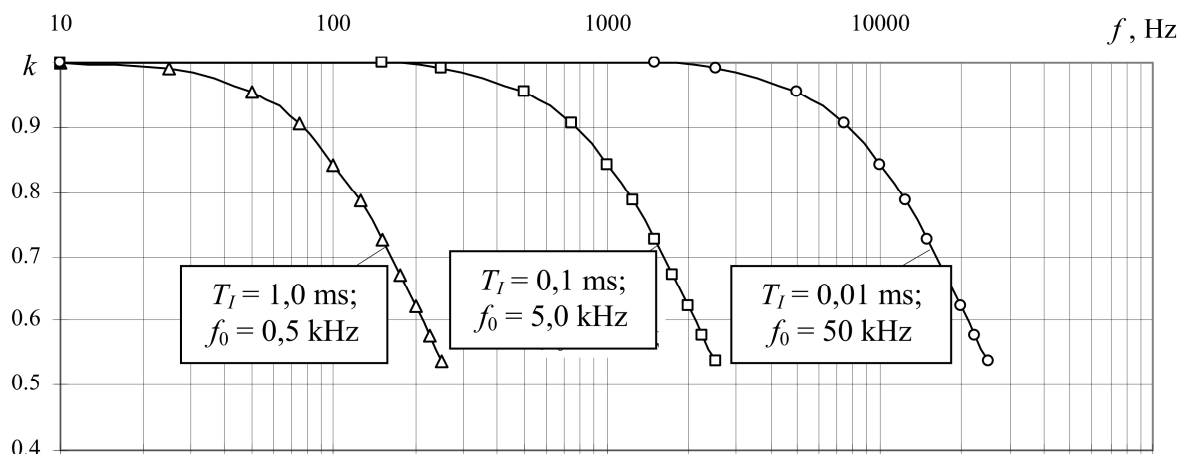


Fig. 7. The logarithmic amplitude-frequency characteristics of the eight-digit integrating ADC – DAC with tactless bit-by-bit equilibration with $\bar{A}_m = |A_m / A_{\max}| = 1,0$ ($A_{\max} = 12,75$ V, $\Delta = 0,1$ B, $A = 50$ mV, $b = 25$ mV, $Z = 255$)

depends only on the time constant of channel integration, which can be used in particular in control systems with variable cycle data collection and processing.

5. Increase speed the tactless ADCs is possible by changing the channel of integration to the proportional amplifier, with simultaneous breaking the feedback loop, which achieved at the cost of noise immunity and accuracy of the ADC.

References

1. Lebedev E.D., Neymark V.E., Pistrak M.Ya., Slezhanovskiy O.V. *Upravlenie ventilnymi elektropriwodami postoyannogo toka [Control of Rectifier Direct-Current Drive]*, Moscow, 1970, 199 p.
2. Usynin U.S., Grigorev M.A., Vinogradov K.M., Gorozhankin A.N., Chupin S.A. Synchronous Reluctance Machine [Sinkhronnaya reaktivnaya mashina], patent 2346376, 2007.
3. Usynin U.S., Moniuszko N.D., Karavaev G.V., Grigorev M.A. The Electric Drive with the Field Regulated Reluctance Machine, *Bulletin of the South Ural State University. Series "Power Engineering"*, 2001, no. 4 (4), pp. 70–76.
4. Usynin U.S., Grigorev M.A., Vinogradov K.M., Gorozhankin A.N. Specific Indicators of the Electric Drive with The Field Regulated Reluctance Machine, *Bulletin of the South Ural State University. Series "Power Engineering"*, 2008, no. 11 (111), pp. 52–53.
5. Bissell, C. Vladimir Aleksandrovich Kotelnikov: Pioneer of the Sampling Theorem, Cryptography, Optimal Detection, Planetary Mapping History of Communications, *Communications Magazine, IEEE*, 2009, № 10, pp. 24–32.
6. Brinkis K., Staltmanis A. The Automated Control of a Power System. *Baltic electrical engineering reviver*, no. 2(6), 1997, pp. 39–44.
7. Osipov O.I., Usynin Yu.S. *Promyshlennyye pomekhi i sposoby ikh podavleniya v ventilnykh elek-*

troprivodakh postoyannogo toka [Industrial Noise and Ways of Their Suppress in Valve DC Electric Drives], Moscow, 1979, 80 p.

8. Pryanishnikov V.A. *Integriruyushchie tsi-frovye voltmetry postoyannogo toka [Integrating digital voltmeters of a direct current]*, Leningrad, 1976, 315 p.

9. Volovich G.I. *Skhemyechnika analogovykh i analogo-tsyfrovykh elektronnykh ustroystv [Circuit design of analog and analog-to-digital electronic devices]*, Moscow, 2005, 459 p.

10. Martyashin A.I., Shakhov E.K., Shlyandin V.M. *Preobrazovateli elektricheskikh parametrov dlya system kontrolya i izmereniya [Converters of Electrical Parameters for Systems to Control and Measurement]*, Moscow, 1976, 390 p.

11. Dudkin M.M., Tsytovich L.I. *Elementy informatsionnoy elektroniki system upravleniya ventilnymi preobrazovatelyami [Elements of Informational Electronics of Control Systems of the Valve Converters]*, Chelyabinsk, 2011, 362 p.

12. Grigorev M.A., Bychkov A.E. The Linear Density of the Surface Current in the Energy-saving Motor Drives with the Field Regulated Reluctance Machine, *Bulletin of the South Ural State University. Series "Power Engineering"*, 2010, no. 32 (208), pp. 46–51.

13. Usynin U.S., Grigorev M.A., Shishkov A.N., Bychkov A.E., Belousov E.V. The Development of Methods for the Synthesis of Frequency Drives with Synchronous Machines, *Bulletin of the South Ural State University. Series "Power Engineering"*, 2011, no. 34 (251), pp. 21–27.

14. Usynin U.S., Grigorev M.A., Shishkov A.N. The Frequency Response of the Torque Control Channel in Synchronous Electric Drive, *Electrical Technology Russia*, 2012, no 4, pp. 54–59.

15. Tsytovich L.I., Dudkin M.M., Kachalov A.V., Rakhmatulin R.M. Reverse Number-Pulse Analogue-to-Digital Converter. [Reversivnyy chislo-impulsnyy analo-

go-tsyfrovooy preobrazovatel], patent 2429563 Russian Federation, publ. 20.09.11, bul. no. 26.

16. Tsytovich L.I., Gafiatullin R.H., Husainov R.Z., Dudkin M.M. Analysis of Dynamics the Integrating Amplitude-Frequency-Pulse Sweep Converter of Analog Signals into Frequency of Pulses, *Bulletin of South Ural State University. Series Power Engineering*, 2003, no.11 (27), pp. 36–40.

17. Tsytovich L.I., Dudkin M.M., Kachalov A.V., Tereshchina O.G., Loginova N.A. Integrating Sweep Converter with Heightened Temperature Stability of Performances, *Pribory i sistemy. Ypravlenie, control, diagnostika*, 2010, no. 10, pp. 38–43.

18. Lokhov S.P., Tsytovich L.I., Dudkin M.M.,

Rakhmatulin R.M., Brylina O.G. "Analogue-Digital-Analogue" Integrating Converter [Inegriruyushchii preobrazovatel "Analog-Tsifro-Analog"], patent 2460210 Russian Federation, publ. 27.08.12, bul. no 24.

19. Lokhov S.P., Tsytovich L.I., Dudkin M.M., Rakhmatulin R.M., Brylina O.G. Closed Integrating Analog-to-Digital Converter with Tactless Bit-by-Bit Equilibration, *Pribory i sistemy. Ypravlenie, control, diagnostika*, 2012, no.11, pp. 27–35.

20. Lokhov S.P., Tsytovich L.I., Dudkin M.M., Brylina O.G., Rakhmatulin R.M. About New Principle of Integrating Analog-to-Digital Conversion with Tactless Bit-by-Bit Equilibration, *Bulletin of South Ural State University. Series Power Engineering*, 2012, no. 37 (296), pp. 97–106.

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О ДИНАМИКЕ НЕКОТОРЫХ СПОСОБОВ ИНТЕГРИРУЮЩЕГО ПРЕОБРАЗОВАНИЯ АНАЛОГОВОГО СИГНАЛА В ЦИФРОВОЙ КОД

Л.И. Цытович, М.М. Дудкин, С.П. Лохов, О.Г. Брылина

Рассмотрены новые принципы построения тактируемых реверсивных интегрирующих аналого-цифровых преобразователей (АЦП) с широтно-импульсной (ШИМ), синфазной амплитудно-частотно-импульсной модуляцией (АЧИМ), а также замкнутого интегрирующего АЦП с бестактовым поразрядным уравновешиванием. Приведены структурные схемы и временные диаграммы сигналов АЦП, дан анализ их динамических характеристик.

Показано, что расширение полосы пропускания АЦП с ШИМ возможно за счет увеличения числа циклов развертывающего преобразования «внутри» интервала синхронизации. В частности, доказано, что АЦП с синфазной АЧИМ по сравнению с известными техническими решениями имеет не менее, чем на порядок более высокую температурную и временную стабильность характеристик. Полоса пропускания в замкнутом интегрирующем АЦП с бестактовым поразрядным уравновешиванием зависит только от постоянной времени канала интегрирования. Значительное расширение полосы пропускания АЦП, приобретаемого ценой снижения метрологических характеристик, возможно в его разомкнутой структуре при отсутствии канала интегрирования.

Ключевые слова: интегрирующий аналого-цифровой преобразователь, интегрирующий развертывающий преобразователь, преобразователь напряжения в частоту импульсов, широтно-импульсная модуляция, амплитудно-частотно-импульсная модуляция, бестактовое поразрядное уравновешивание, помехоустойчивость, система управления.

Литература

1. Управление вентильными электроприводами постоянного тока / Е.Д. Лебедев, В.Е. Неймарк, М.Я. Пистрак, О.В. Слежановский. – М.: Энергия, 1970. – 199 с.
2. Пат. 2346376 Российская Федерация, МПК Н 02 К 19/24. Синхронная реактивная машина / Ю.С. Усынин, М.А. Григорьев, К.М. Виноградов, А.Н. Горожанкин, С.А. Чупин. – № 2007126685; заявл. 12.07.07; опубл. 10.02.09, Бюл. № 4.
3. Электропривод с синхронным реактивным двигателем независимого возбуждения / Ю.С. Усынин, Н.Д. Монюшко, Г.В. Караваев, М.А. Григорьев // Вестник ЮУрГУ. Серия «Энергетика». – 2001. – Вып. 1. – № 4(4). – С. 70–76.

4. Удельные показатели электропривода с синхронным реактивным двигателем независимого возбуждения / Ю.С. Усынин, М.А. Григорьев, К.М. Виноградов, А.Н. Горожанкин // Вестник ЮУрГУ. Серия «Энергетика». – 2008. – Вып. 9. – № 11(111). – С. 52–53.
5. Bissell, C. Vladimir Aleksandrovich Kotelnikov: pioneer of the sampling theorem, cryptography, optimal detection, planetary mapping ... History of Communications / C. Bissell // Communications Magazine. IEEE. – 2009. – № 10. – P. 24–32.
6. Brinkis, K. The automated control of a power system / K. Brinkis, A. Staltmanis // Baltic electrical engineering review. – 1997. – № 2(6). – P. 39–44.
7. Осипов, О.И. Промышленные помехи и способы их подавления в вентильных электроприводах постоянного тока / О.И. Осипов, Ю.С. Усынин. – М.: Энергия, 1979. – 80 с.
8. Прянишников, В.А. Интегрирующие цифровые вольтметры постоянного тока / В.А. Прянишников. – Л.: Энергия, 1976. – 315 с.
9. Волович, Г.И. Схемотехника аналоговых и аналогово-цифровых электронных устройств / Г.И. Волович. – М.: Издательский дом «Додэка-XXI», 2005. – 459 с.
10. Мартяшин, А.И. Преобразователи электрических параметров для систем контроля и измерения / А.И. Мартяшин, Э.К. Шахов, В.М. Шлядин. – М.: Энергия, 1976. – 390 с.
11. Дудкин, М.М. Элементы информационной электроники систем управления вентильными преобразователями: монография / М.М. Дудкин, Л.И. Цытович. – Челябинск: Издательский центр ЮУрГУ, 2011. – 362 с.
12. Григорьев, М.А. Линейная плотность поверхностного тока в энергосберегающих электроприводах с синхронной реактивной машиной независимого возбуждения / М.А. Григорьев, А.Е. Бычков // Вестник ЮУрГУ. Серия «Энергетика». – 2010. – Вып. 14. – № 32(208). – С. 46–51.
13. Развитие частотных методов синтеза электроприводов с синхронными электрическими машинами / Ю.С. Усынин, М.А. Григорьев, А.Н. Шишков и др. // Вестник ЮУрГУ. Серия «Энергетика». – 2011. – Вып. 16. – № 34(251). – С. 21–27.
14. Частотные характеристики канала регулирования момента в синхронных электроприводах / Ю.С. Усынин, М.А. Григорьев, А.Н. Шишков // Электричество. – 2012. – № 4. – С. 54–59.
15. Пат. 2429563 Российская Федерация, МПК7 Н 03 М 1/02. Реверсивный число-импульсный аналого-цифровой преобразователь / Л.И. Цытович, М.М. Дудкин, А.В. Качалов, Р.М. Рахматулин. – № 2009147981/09; заявл. 23.12.09; опубл. 20.09.11, Бюл. № 26.
16. Анализ динамики интегрирующего амплитудно-частотно-импульсного развертывающего преобразователя аналоговых сигналов в частоту импульсов / Л.И. Цытович, Р.Х. Гафиятуллин, Р.З. Хусаинов, М.М. Дудкин // Вестник ЮУрГУ. Серия «Энергетика». – 2003. – Вып. 3. – № 11(27). – С. 36–40.
17. Интегрирующие развертывающие преобразователи с повышенной температурной стабильностью характеристик / Л.И. Цытович, М.М. Дудкин, А.В. Качалов и др. // Приборы и системы. Управление, контроль, диагностика. – 2010. – № 10. – С. 38–43.
18. Пат. 2460210 Российская Федерация. МПК7 Н 03 М 1/52. Интегрирующий преобразователь «Аналог – Цифра – Аналог» / С.П. Лохов, Л.И. Цытович, М.М. Дудкин, Р.М. Рахматуллин, О.Г. Брылина. – № 2011125193/08; заявл. 17.06.11; опубл. 27.08.12, Бюл. № 24.
19. Замкнутый интегрирующий аналого-цифровой преобразователь с бестактовым поразрядным уравниванием / С.П. Лохов, Л.И. Цытович, М.М. Дудкин и др. // Приборы и системы. Управление, контроль, диагностика. – 2012. – № 11. – С. 27–35.
20. О новом принципе интегрирующего аналого-цифрового преобразования с бестактовым поразрядным уравниванием / С.П. Лохов, Л.И. Цытович, М.М. Дудкин и др. // Вестник ЮУрГУ. Серия «Энергетика». – 2012. – Вып. 18. – № 37 (296). – С. 97–106.

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